Constant Maximum Throughput Power in Multisync Monitor SMPS Based on the L5993 PWM Controller

C. ADRAGNA, M. FAGNANI
SGS-THOMSON Microelectronics - via C. Olivetti, 2 - 20041 Agrate Brianza (MI), Italy

Abstract

In multisync monitors the operating frequency of the SMPS (Switched Mode Power Supply), typically realized with a flyback converter, is usually synchronized to the raster line scan signal of the display, to reduce the effect of the noise generated. The switching frequency of the converter can range therefore from about 30 kHz up to 90 kHz and above, depending on the monitor and its operating conditions.
In case of overload, the power delivered by such a converter increases considerably with the switching frequency, despite current mode control provides inherent current limitation.
This paper describes a control circuit able to limit the throughput power of an overloaded flyback converter independently of its switching frequency. Furthermore, it deals with the implementation of this control on the SGS-THOMSON's integrated controller L5993.

1 Introduction

Overcurrent protection, a safety feature almost always required in switching converters, allows to optimize the magnetic and power semiconductor elements as well as to ensure a safe and reliable operation.
The fixed frequency "peak" current mode control scheme, illustrated in fig. 1, contains an inherent pulse-by-pulse current limiting and provides an easy way to set an upper limit on the peak of the current flowing through the power switch. In general, such a limitation sets also the maximum power capability of the converter.

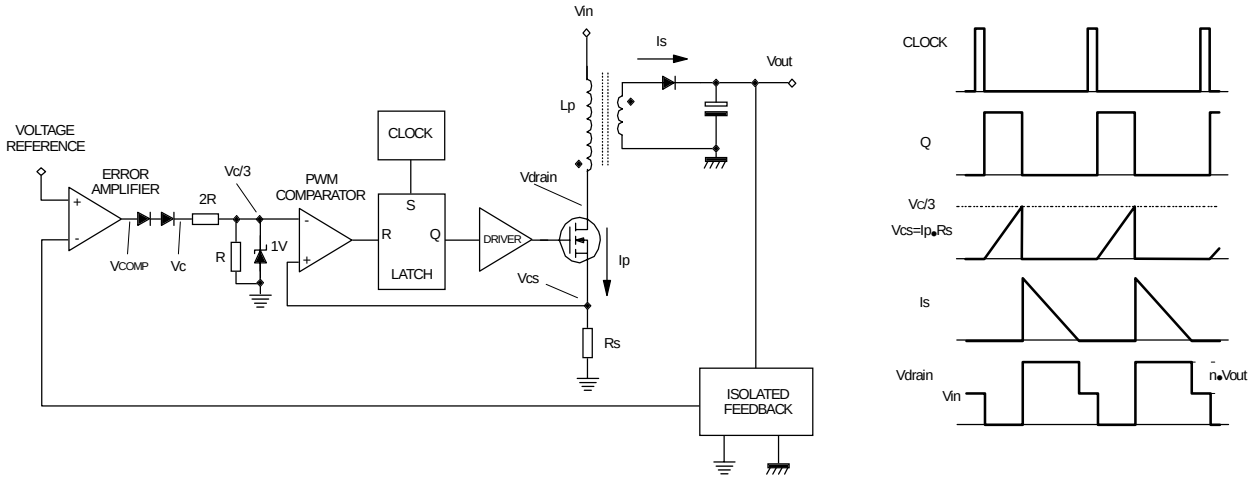

Fig. 1. Flyback converter topology with peak current mode control and associated waveforms.

From the schematic of fig. 1 and the relevant waveforms, it is possible to see that the conduction of the power switch is terminated as the voltage on the (+) input of the PWM comparator (given by the instantaneous value of I_p times R_s) reaches the voltage applied on the (-) input.
Limiting this voltage to a maximum value (1 V) means putting the same limit on the voltage on the (+) input, that is limiting the peak value of the input current (I_{px}) to $I_{px\max} = 1/R_s$. The maximum input power will be then limited to $P_{in\max}$, a value somehow related to $I_{px\max}$.
Practically, if the peak input current needed to supply the load is greater than $I_{px\max}$, the converter will be unable to deliver such a current and will go out of regulation (i.e. the output voltage will drop from its regulated value). The power drawn from the input source will not exceed $P_{in\max}$ and, obviously, the output power will be in turn limited.

Resolution	Refresh rate	Horizontal Frequency	Standard Type
640 x 350	70 Hz	31.5 kHz	Industry
	85 Hz	37.9 kHz	VESA
640 x 400	85 Hz	37.9 kHz	VESA
720 x 400	70 Hz	31.5 kHz	Industry
	85 Hz	37.9 kHz	VESA
640 x 480	60 Hz	31.5 kHz	Industry
	72 Hz	37.9 kHz	VESA
	75 Hz	37.5 kHz	VESA
	85 Hz	43.3 kHz	VESA
800 x 600	56 Hz	35.2 kHz	Industry
	72 Hz	48.1 kHz	VESA
	75 Hz	46.9 kHz	VESA
	85 Hz	53.7 kHz	VESA
816 x 612	72 Hz	48.1 kHz	Industry
1024 x 768	43 Hz Interl.	35.5 kHz	Industry
	70 Hz	56.5 kHz	VESA
	75 Hz	60.0 kHz	VESA
	85 Hz	68.7 kHz	VESA
1152 x 864	75 Hz	67.5 kHz	VESA
1280 x 960	60 Hz	60.0 kHz	VESA
	85 Hz	85.9 kHz	VESA
1280 x 1024	60 Hz	64.0 kHz	Industry
	75 Hz	80.0 kHz	VESA
	85 Hz	91.1 kHz	VESA

Tab. 1 - VESA and common Industry Standards for Computer Display Monitor

Despite the ultimate aim of such a protection is to limit the power capability of the converter, that is the maximum power it can deliver to the output, it is more convenient to refer to the input power since the control is usually exercised on the input side of the converter (primary control).
Generally speaking, the relationship between the peak input current and the input power depends on the converter's topology and its operating mode: DCM (Discontinuous Current conduction Mode) or CCM (Continuous Current conduction Mode). In DCM operation, the switching

frequency (f_{sw}) strongly affects this relationship, whereas in CCM operation this dependence still exists but is less pronounced, the farther from DCM, the less the dependence.
In this context it is important to point out the impact of the switching frequency on the maximum input power thus the discussion will be addressed to flyback converters only. In fact, while flyback converters may be designed to operate in either mode, forward and forward-derived converters are practically always designed to operate in CCM, usually far from the boundary with DCM.
It is useful to consider again the example of fig. 1 (a flyback converter operating in DCM). In this system the maximum input power is given by:

$$P_{in\,\max} = \frac{1}{2} \bullet L_p \bullet I_{px\,\max}^2 \bullet f_{sw} \quad (1)\,,$$

where L_p is the primary inductance of the transformer.
Equation (1) states that the maximum input power is proportional to the switching frequency, for a fixed peak input current $I_{px\max}$. For instance, if the switching frequency is doubled the power capability of the flyback will be doubled as well (provided it is still working in DCM).
In numerous applications, the SMPS switching frequency does not change: it has a constant value imposed by the frequency of an oscillator usually embodied in the controller and programmed by means of external passive parts (usually, an RC group).
However, in monitor power supplies (where flyback topology is the preferred one) the switching frequency is often locked to the raster line scan signal of the display, in order to increase the noise immunity. If the monitor is a multisync type the line scan frequency will change in a certain range (as shown in Tab. 1 where some VESA and common industry standards are summarized) and so will do also the SMPS switching frequency. As a consequence, also the SMPS power capability will considerably vary.
The resistor R_s (which fixes the current limiting setpoint) will be selected so that the capability is enough to supply the maximum power required by the load at the minimum operating frequency.
In case of a load failure (i.e. a short circuit), at minimum frequency the current limiting circuit will be tripped, thus the converter will go out of regulation and a power slightly greater than the full load one will be drawn from the input source (and delivered to the load).
Instead, at maximum frequency, a power by far larger has to circulate before tripping the current limiting. In the interests of safety, the design of the SMPS should be based on this maximum capability but this is clearly a significant increase both in terms of cost and overall physical size.

2 Flyback and Current Mode Control Basics

Before going through the solution proposed to solve this problem, it is useful to remind some basic relationships describing the operation of flyback topology as well as of "peak" current mode control based on the architecture shown in fig. 1 and implemented by numerous PWM controllers such as the popular UC384x.
Flyback's operation takes place in a two-step process. During the ON time of the switch, energy is taken from the input and stored in the primary of the flyback transformer (actually, two coupled inductors). At the secondary side, the catch diode is reverse-biased, thus the load is being supplied by the energy stored in the output bulk capacitor.
When the switch turns off, the primary circuit is open and the energy stored in the primary is transferred to the secondary by magnetic coupling. The catch diode is forward-biased, and the

stored energy is delivered to the output capacitor and to the load. The output voltage is reflected back to the primary through the turns ratio and adds up to the input one, giving origin to a high voltage on the switch.
Flyback topology is operating in DCM when the input (or primary) current starts from zero at the beginning of a given switching cycle. This happens because the secondary of the transformer has discharged all the energy stored in the previous period. If this energy transfer is not complete, then the primary current will start from a value greater than zero at the beginning of each cycle and the flyback is said to be operating in CCM. DCM is then characterized by currents shaped in a triangular fashion, whereas CCM features trapezoidal currents.
As to flyback topology operating in DCM, the relationship between the peak input current (*Ipx*) and the input power (*Pin*) is:

$$I_{px(DCM)} = \sqrt{\frac{2 \bullet P_{in}}{L_p \bullet f_{sw}}} \quad (2)\,.$$

The point is: in a given flyback, when operating in DCM, the peak input current depends solely on the power drawn from the input.
In CCM operation this relationship becomes:

$$I_{px(CCM)} = \frac{P_{in}}{V_E} + \frac{V_E}{2 \bullet f_{sw} \bullet L_p} \quad (3)\,,$$

where the "equivalent input voltage" V_E is defined as follows:

$$V_E = \frac{V_{in}}{1 + \frac{V_{in}}{n \bullet V_{out}}} \quad (4)\,.$$

The equivalent input voltage V_E can be considered as a function of the DC input voltage (*Vin*) only, since the regulated output voltage (*Vout*) is a design spec and the primary-to-secondary turns ratio (*n*) is fixed with considerations on the breakdown voltage of the switch ($n \bullet Vout$ is the voltage reflected back to the primary). Fig. 2 shows the diagram of eqn. (4) while Tab. 2 presents the ranges of V_E relevant to typical mains voltages.

Mains [Vac]		110 ± 20%	220/230 ± 20%	Universal
Vin range [Vdc]		100 ÷ 175	215 ÷ 370	100 ÷ 385
V_E range [Vdc]	$n \bullet Vout$ = 50	**33.3 ÷ 38.9**	**40.6 ÷ 44.0**	**33.3 ÷ 44.3**
	$n \bullet Vout$ = 100	**50.0 ÷ 63.6**	**68.3 ÷ 78.7**	**50.0 ÷ 79.4**
	$n \bullet Vout$ = 150	**60.0 ÷ 80.8**	**88.4 ÷ 106.7**	**60.0 ÷ 107.9**
Conditions: 30% ripple overimposed on DC value @ *Pin=Pin*max, *Vin=Vin*min				

Tab. 2 - V_E ranges for different mains and reflected voltages

Eqn. 3 shows that CCM operation implies the dependence of the peak input current on both the input power and the input voltage.

The boundary between these two types of operation depends on several parameters. Some of them are structural, that is parameters that identify the flyback converter: inductance of the primary of the transformer, transformer turns ratio and regulated output voltage. Others are related to the external world and are subject to changes: input voltage and output load. The switching frequency, in this context, can vary according to an external signal thus it will be considered being part of the external world parameters.

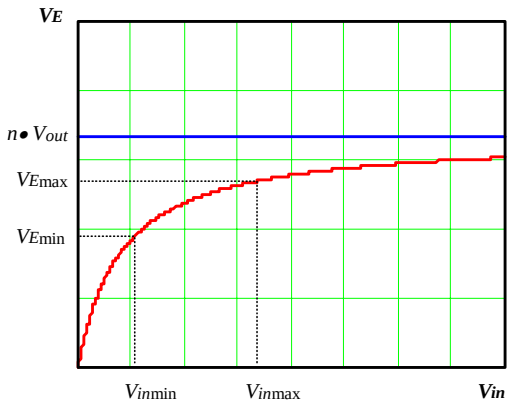

Fig.2 - Equivalent Input Voltage as a function of *Vin*

In order to characterize the transition from one mode to the other, it is useful to define:

- the Transition Power (P_{inT}) that is the maximum input power at which a given flyback works in DCM (or rather the minimum input power at which a given flyback works in CCM) for a given input voltage and a given switching frequency:

$$P_{inT} = \frac{V_E^2}{2 \bullet f_{sw} \bullet L_p} \qquad (5)$$

  (DCM will take place for $P_{in} < P_{inT}$ and CCM for $P_{in} > P_{inT}$);
- the Transition Voltage (V_{ET}) that is equivalent input voltage at which the operation is on the boundary between DCM and CCM for a given input voltage and a given switching frequency:

$$V_{ET} = \sqrt{2 \bullet f_{sw} \bullet L_p \bullet P_{in}} \qquad (6)$$

  (DCM will take place for $V_E > V_{ET}$ and CCM for $V_E < V_{ET}$);
- the Transition Frequency (f_T) that is the switching frequency at which the transition between DCM and CCM (and vice versa), for a given input equivalent voltage and a given input power, takes place:

$$f_T = \frac{V_E^2}{2 \bullet L_p \bullet P_{in}} \qquad (7)\,.$$

  (DCM will take place for $f_{sw} < f_T$ and CCM for $f_{sw} > f_T$).

This is summarized in fig. 3. Equation (5) is represented on the plane V_E-P_{inT} by a set of parabolas, one for each switching frequency (the dashed one refers to a lower value). The range V_{Emin} - V_{Emax} is defined as sketched in table 1.
An assigned f_{sw} defines the relevant parabola and, therefore, the area of CCM operation (the one above the parabola) and the area of DCM operation (the one below). Thus, for an assigned pair (V_E, P_{in}), it is possible to deduce the operating mode by observing where the representative point is located on the plane.
For a given input power P_{in}, represented by a horizontal line, the intersection with the parabola relevant to the current switching frequency defines the transition voltage V_{ET} given by (6).
Alternatively, an assigned pair (V_E, P_{in}) defines a unique parabola, corresponding to the f_T relevant to that pair as per equation (7).

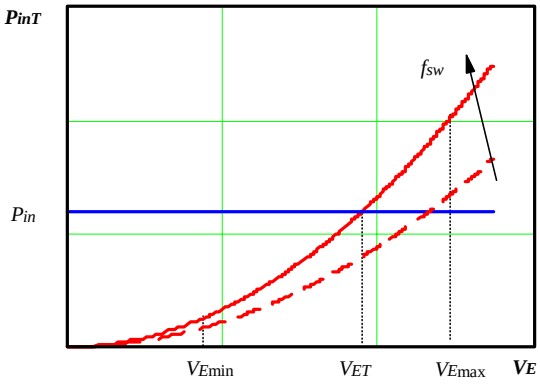

Fig. 3 - Characterization of the transition between DCM and CCM

As to current loop, from the inspection of the equivalent schematic shown in fig.1 it is possible to find the relationship between the peak primary current (I_{px}), the peak voltage (V_{csx}) on the (-) input of the PWM comparator and the output voltage (V_{COMP}) of the error amplifier (E/A):

$$V_{COMP} = V_C + 2 \bullet V_f = 3 \bullet V_{csx} + 2 \bullet V_f = 3 \bullet \left(R_s \bullet I_{px} + V_o \right) + 2 \bullet V_f \qquad (8)$$

where V_f is the forward drop on each "zero duty cycle diode" and V_o a DC offset voltage that might be applied on the (-) input of the PWM comparator (that is on the current sense input of the PWM controller). V_C, the voltage downstream the two zero duty cycle diodes (and applied on the x3 divider), despite not really available, is convenient for future considerations.
Considering the 1V clamp on the (+) input of the current sense comparator, V_C will be included between 0 and 3 V, and the useful swing of V_{COMP} between 2•V_f and 3 + 2•V_f volt.
Actually, equation (8) neglects the so-called “delay to output” of the PWM controller, that is the propagation delay of the current sense path (PWM comparator + latch + driver). During this time, the switch is still ON and the input current keeps on ramping up, despite V_{cs} has already hit the internal level on (-) input of the PWM comparator.
This time lag (T_{DELAY}, typically in the range of 100 ns) is compensated by the voltage loop when the system is regulating: V_{COMP} is slightly lower than the value predicted by (8) (but the phase margin of the control loop gain will be reduced). However, as shown in fig. 4, T_{DELAY} causes the peak current I_{px} to be larger than the expected value when the error amplifier is saturated high and the pulse-by-pulse limiting is tripped.

To account for delay to output, equation (8) should be rewritten as follows:

$$V_{COMP} = 3 \bullet \left[R_s \bullet \left(I_{px} - \Delta I \right) + V_o \right] + 2 \bullet V_f \qquad (9),$$

where the current overflow ΔI is:

$$\Delta I = \frac{V_{in}}{L_p} \bullet T_{DELAY} \qquad (10).$$

Being ΔI proportional to the input voltage, the delay to output can even dramatically change the power capability of the converter, especially in case of large input voltage variations, such as in Universal Mains applications.

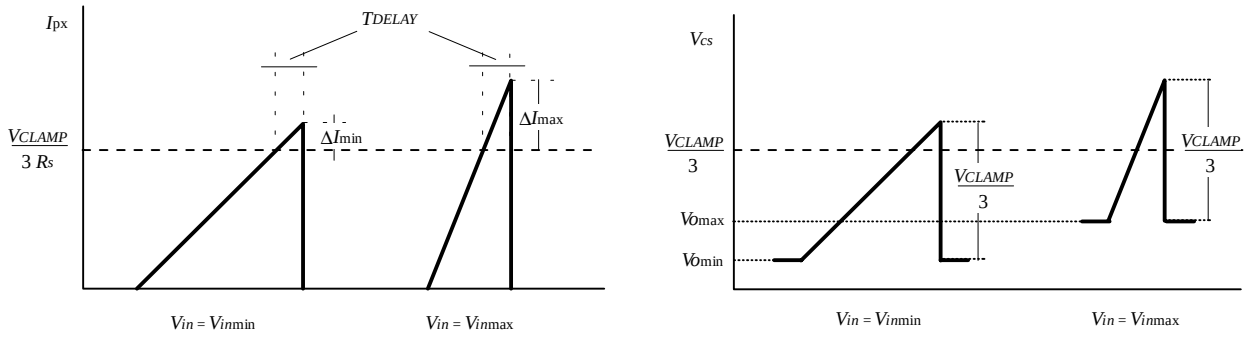

Fig. 4 - Effect of delay to output and its compensation by means of V_O

Anyway, if the offset voltage is selected so that:

$$V_o = V_o' = R_s \bullet \Delta I = R_s \bullet \frac{V_{in}}{Lp} \bullet T_{DELAY} \qquad (11),$$

the term ΔI is canceled in (9) and the effect of the delay to output is eliminated. Equation (8) will still apply, provided V_O is regarded as the difference between the actual offset voltage applied to the current sense input of the PWM controller and the compensating value V'_O.

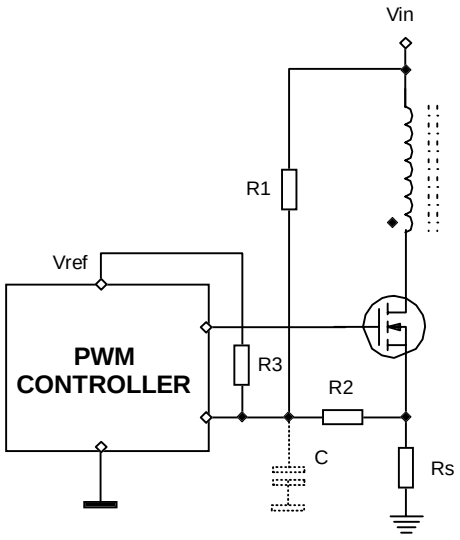

Fig. 5 - Compensation of the internal propagation delay ($R1$) and additional offsetting ($R3$) on current sense

The compensation can be easily realized with the circuit shown in fig. 5. $R2$ is often used along with the capacitor C to smooth the leading edge spikes occuring when the switch turns on (despite the inintial blanking time of the current sense input performed in some controllers). In such a case only $R1$ will be added. Considering that V'_o is in the hundred mV and that, therefore, $R1 >> R2$ ($R2$ is typically 1kΩ, $R1$ is in the MΩ), perfect delay compensation will be achieved when their ratio is:

$$\frac{R2}{R1} = \frac{T_{DELAY}}{L_p} \bullet R_s \quad (12)\,.$$

The resistor $R3$, connected to a voltage reference usually available on-chip, is used if an additional constant offset is required.

3 The Constant Power Function

In principle, to achieve a constant maximum power $P_{in\max}$ on varying the switching frequency it is necessary to reduce the maximum admitted value of the peak current $I_{px\max}$ as frequency builds up and vice versa. To do so there are two possible approaches:

- Offset approach: adding on pin ISEN a DC offset voltage increasing with frequency, so that the I_{px} value needed for V_{csx} to reach 1V is reduced.
- Clamp approach: clamping V_{COMP} (or V_C) to a value which decreases as frequency increases.

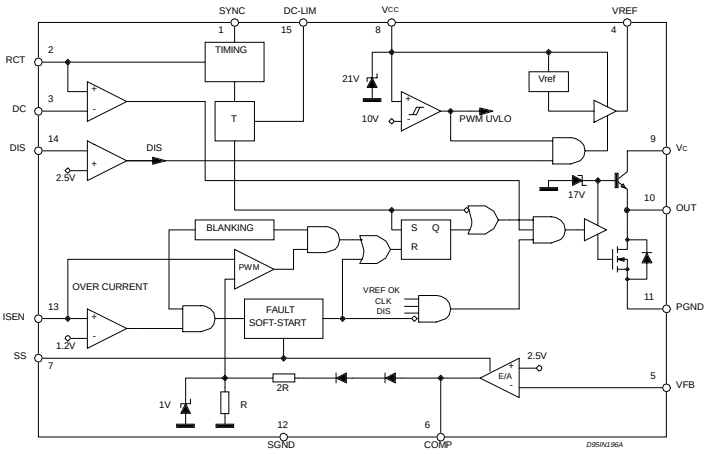

Fig. 6 - SGS-THOMSON's L4990 internal block diagram

In both cases it is necessary to generate a voltage level whose dependence on frequency is non-linear. Besides, the target is to add the "Constant Power" function on-board to an existing device which is housed in a 16 pin package, with only one available pin. This requires this voltage to be independent of shape, amplitude and duration of the synchronization pulses, parameters that depend on the specific application.

The device where the function is to be integrated is SGS-THOMSON's current mode PWM controller L4990, whose internal block diagram is shown in fig. 6.

Synchronising the oscillator of the L4990 to an external signal $f_{sync} \in [f_{min}, f_{max}]$ implies firstly that the signal is to be fed into pin 1 (SYNC), after an appropriate conditioning if necessary. In the second place, the free-running frequency of the oscillator (f_{osc}) is set to a value slightly lower than f_{min} (typically, 10-20%) to take account of tolerances. Finally, the amplitude of the sawtooth generated (which swings between 1 and 3 V when free-running) diminishes as frequency rises, because of the reduction of the peak value V_{pk} as shown in fig. 7.

Neglecting the fall time of the sawtooth, it is possible to find that the peak voltage depends on the synchronizing frequency according to the following relationship:

$$V_{pk} = 5 - 2^{\left(2 - \frac{f_{osc}}{f_{sync}}\right)} \qquad (13)$$

whose diagram is shown in fig. 8.

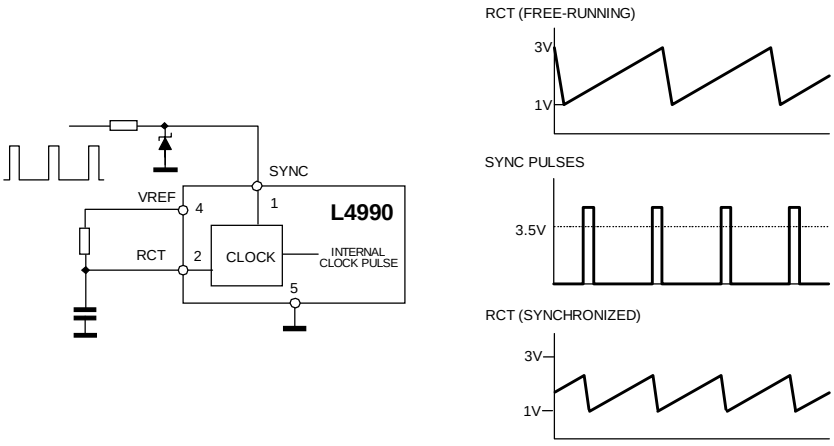

Fig. 7 - L4990 oscillator synchronization

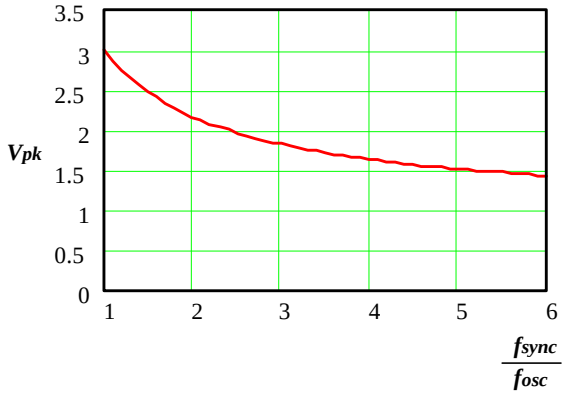

Fig. 8 - Oscillator peak amplitude vs. f_{sync} / f_{osc}

A peak-holding circuit (see fig. 9) made up of a diode, a capacitor and a resistor, separated by a buffer so as not to alter the free-running frequency of the oscillator, is used to detect the oscillator sawtooth peak value.
The voltage on the capacitor C will be a DC level $V_H = V_{pk} - V_f$, provided the resistor R, which allows V_H to diminish when the synchronization frequency increases, is such that the RC time constant, is much higher than 1 / f_{osc}.
With this technique V_H will be independent of shape, amplitude and duration of the syncronization pulses, as required.

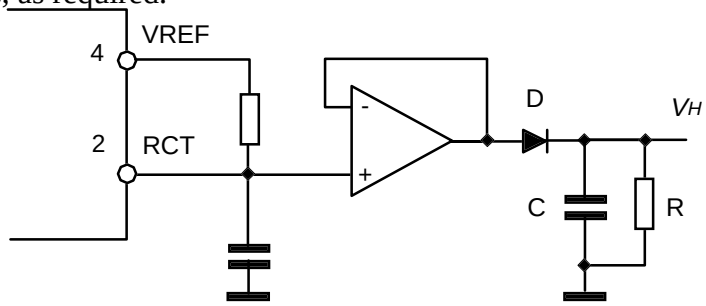

Fig. 9 - Frequency-to-voltage converter based on oscillator peak voltage detection.

In present multisync monitors f_{min} is around 30 kHz (refer also to Tab. 1), thus it reasonable to assume the oscillator free-running frequency to be ≈25 kHz. This means that the time constant of the RC group should be in the ms and that the available pin of the L4990 needs be used to connect the capacitor of the peak-holding circuit externally, since the capacitance values required are not feasible on-chip.
V_H might be used for both the above mentioned approaches, as shown in fig. 10, but the clamp approach is clearly simpler and more straightforward because the range of V_H fits the dynamics of V_C (and the one of V_{COMP}, except two diode forward drop). In fact, the PNP clamps the emitter voltage one V_{be} above V_H, thus the drop on the diode D can be compensated.

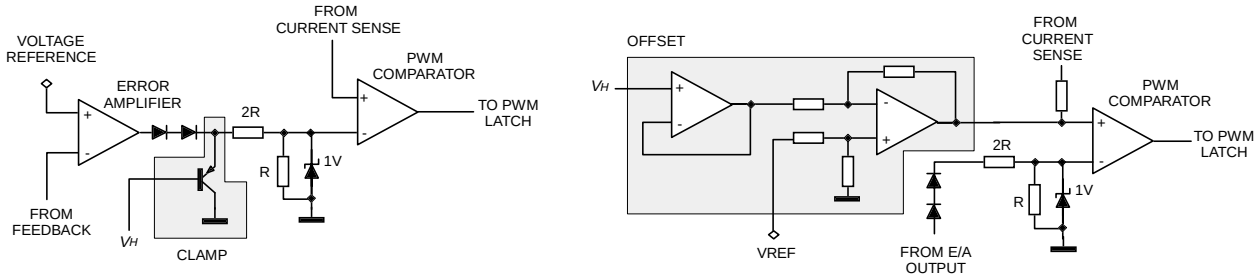

Fig. 10 - Circuits for using the circuit of fig. 9 with Clamp (a) and Offset (b) approaches

In order to understand whether this solution is practicable, the still open point is to check the correction realized by clamping V_C to V_{pk} for producing small variations of $P_{in\max}$ over the entire frequency range [$f_{min} < f_{sync} < f_{max}$].
In other words, the "Actual Correction Law" (ACL), whose theoretical expression is given by (13), is to be compared with the "Ideal Correction Law" (ICL), obtained by substituting (8) in (2) and (3):

$$V_{CLAMP} = \begin{cases} 3 \bullet \left(R_s \bullet \sqrt{\dfrac{2 \bullet P_{in\max}}{f_{sync} \bullet L_p}} + V_o \right) & , f_{sync} < f_T \\ 3 \bullet \left[R_s \bullet \left(\dfrac{P_{in\max}}{V_E} + \dfrac{V_E}{2 \bullet f_{sync} \bullet L_p} \right) + V_o \right] & , f_{sync} \geq f_T \end{cases} \quad (14),$$

where the transition frequency f_T, according to (7), is defined as:

$$f_T = \frac{V_E^2}{2 \bullet L_p \bullet P_{in\max}} \quad (15),$$

and V_o is an offset added, in case, to the one (V'_o) necessary to compensate the delay to output of the controller.
The sense resistor R_s should be selected so that V_{CLAMP} = 3V @ f_{sync} / f_{osc} = 1 and $V_E = V_{E\min}$.. In this way, when the oscillator is free-running (in the absence of the synchronization signal), the Constant Power clamp circuit will not interfere with the 1V default clamp in any case.
To evaluate the discrepancy between ICL (14) and the theoretical ACL (13), some manipulations, illustrated in appendix A, are necessary. The final result is:

$$V_{CLAMP} = \begin{cases} \begin{cases} 3 \bullet \left[\dfrac{2 \bullet (1 - V_o)}{1 + k} \bullet \sqrt{k \bullet \dfrac{f_{osc}}{f_{sync}}} + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} < k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \\ 3 \bullet \left[\dfrac{1 - V_o}{1 + k} \bullet \left(\dfrac{V_{E\min}}{V_E} + k \bullet \dfrac{V_E}{V_{E\min}} \bullet \dfrac{f_{osc}}{f_{sync}} \right) + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \geq k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \end{cases} & , \ k \leq 1 \\ \begin{cases} 3 \bullet \left[(1 - V_o) \bullet \sqrt{\dfrac{f_{osc}}{f_{sync}}} + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} < k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \\ 3 \bullet \left[\dfrac{1 - V_o}{2 \bullet \sqrt{k}} \bullet \left(\dfrac{V_{E\min}}{V_E} + k \bullet \dfrac{V_E}{V_{E\min}} \bullet \dfrac{f_{osc}}{f_{sync}} \right) + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \geq k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \end{cases} & , \ k > 1 \end{cases} \quad (16),$$

where k, for consistency with equation (13), is defined as:

$$k = \frac{f_{T\min}}{f_{osc}} \quad (17),$$

being $f_{T\min}$ the minimum transition frequency (@ $Pin = Pin\max$):

$$f_{T\min} = \frac{V_{E\min}^2}{2 \bullet L_p \bullet P_{in\max}} \quad (18).$$

With this position, k plays the role of a characteristic parameter of flyback converters, indicating their prevailing operation mode: the lower is k, the more the converter operates in CCM and, vice versa, higher values of k indicate a shift towards DCM. Selecting a value for k ultimately means selecting the value of Lp:

$$L_p = \frac{V_{E\min}^2}{2 \bullet k \bullet f_{osc} \bullet P_{in\max}} \quad (19).$$

As required earlier, equations (16) have been derived under the assumption that Rs is such that $V_{CLAMP} = 3V$ @ $f_{sync} / f_{osc} = 1$ and $V_E = V_{E\min}$. Its value is therefore:

$$Rs = \begin{cases} \dfrac{(1 - V_o) \bullet V_{E\min}}{(1 + k) \bullet P_{in\max}} & , \ k \leq 1 \\ \dfrac{(1 - V_o) \bullet V_{E\min}}{2 \bullet \sqrt{k} \bullet P_{in\max}} & , \ k > 1 \end{cases} \quad (20).$$

Ultimately, equations (16) will be compared to equation (13) considering different values of k and of the ratio $h = V_E / V_{E\min}$.
As to the range of h, it can be derived from the data of Tab.2 and is shown in Tab. 3,

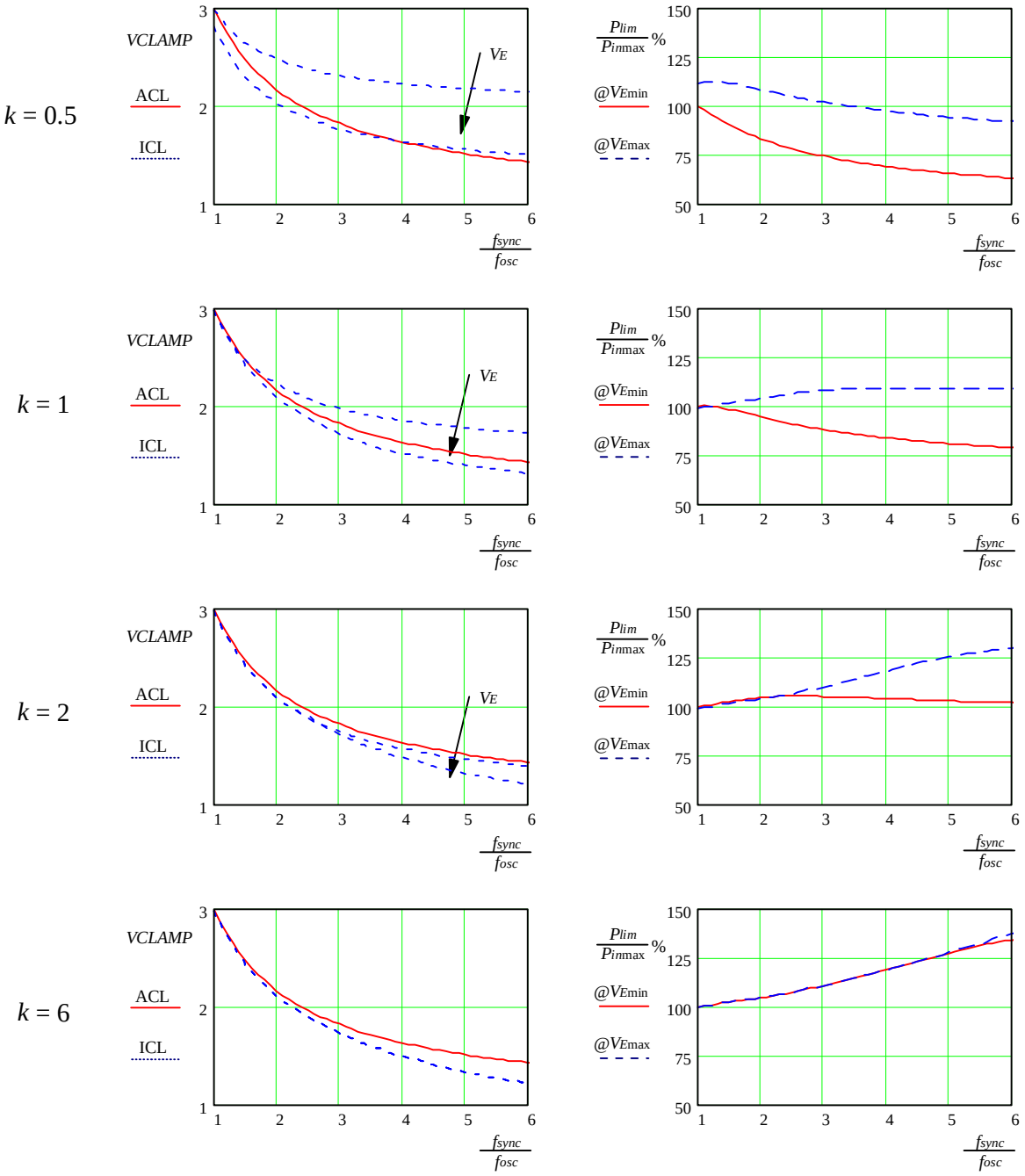

Fig. 11 - Comparison between ICL and the theoretical ACL (Universal Mains)

Mains [Vac]		110 ± 20%	220/230 ± 20%	Universal
	$n \bullet V_{out}$ = 50	**1 ÷ 1.17**	**1 ÷ 1.09**	**1 ÷1.33**
h range	$n \bullet V_{out}$ = 100	**1 ÷ 1.27**	**1 ÷ 1.15**	**1 ÷1.59**
	$n \bullet V_{out}$ = 150	**1 ÷ 1.35**	**1 ÷ 1.21**	**1 ÷ 1.80**

Tab. 3 - Range of parameter h for different mains voltages

The range of k is top bounded by f_{max} / f_{osc}: in fact, if $f_{Tmin} > f_{max}$ the system will always operate in DCM thus ICL will no longer change, even by further increasing k.

As previously shown in Tab. 1, in the majority of the present applications f_{max} / f_{min} does not exceed 3. Currently, however, some advanced projects are enlarging this range, thus a maximum value of 6 will be assumed for f_{max} / f_{osc} and, therefore, for k.
The results of the comparison is summarized in the diagrams of fig. 11. They refer to a Universal Mains input (which covers the other cases) and have been drawn considering the range of V_E that corresponds to 100V reflected voltage (which is a value most commonly used) and no additional offset on current sense (V_O = 0).
On the left column, the solid curve indicates ACL while the dotted ones represent ICL at the extreme values of V_E. On the right column, it is shown the ratio between the actual maximum input power P_{lim} and the desired limit $P_{in\,max}$, resulting from ACL, at minimum (solid line) and maximum (dashed line) V_E.
When the system is shifted towards CCM ($k \leq 0.5$) ICL is very sensitive to variations of V_E. ACL is very heavy and limits the power capability well below the desired value, especially at $V_E = V_{E\,min}$ and in the higher frequency range. Things, of course, would even worsen if we considered lower values of k. On the other hand a correction would no longer be necessary if the sytem was shifted further towards CCM.
For k = 1 the system is "quite CCM" and the correction, although good at $V_E = V_{E\,max}$ (especially in the 1:3 range of f_{sync} / f_{osc}), is still too heavy at $V_E = V_{E\,min}$. ICL is now less dependent on V_E.
A good fit appears to be when k is in the neighbourhood of 2 at $V_E = V_{e\,min}$.
For k = 6 there is no significant difference between the behaviour at $V_{E\,min}$ and $V_{E\,max}$: ICL is no longer dependent on V_E because the system is always working in DCM. The correction is good in the 1:3 f_{sync} / f_{osc} range but worsens at f_{sync} / f_{osc} = 6.
Although these comments apply to the theoretical ACL they can be used as a starting point of the investigation once the real ACL will be determined.

4 The L5993 PWM controller

SGS-THOMSON's L5993 current mode PWM controller incorporates the "Constant Power" function along with the other ancillary functions already available on its ancestor L4990, such as input/output synchronization, maximum duty cycle control, programmable soft-start, overcurrent protection with restart delay, latched disable and internal leading edge blanking on current sense. In addition, it features significant improvements as to the start-up current (<150 µA), the precision of the reference (2% including temperature) and the delay to output (70 µA typ.). The internal block diagram is shown in fig. 12.
The external capacitor needed to complete the peak-holding circuit is connected between pin 16 (C-POWER) and ground. Since the internal resistor that discharges the capacitor in case of frequency decrease is 47 kΩ (±30%), the minimum capacitance value (C), in order to have less than 1% ripple superimposed on the DC voltage, should be:

$$C > \frac{1}{330 \bullet f_{osc}} \qquad (21)$$

If pin 16 is connected to pin 4 (Vref) the clamp and the Constant Power function will be disabled.

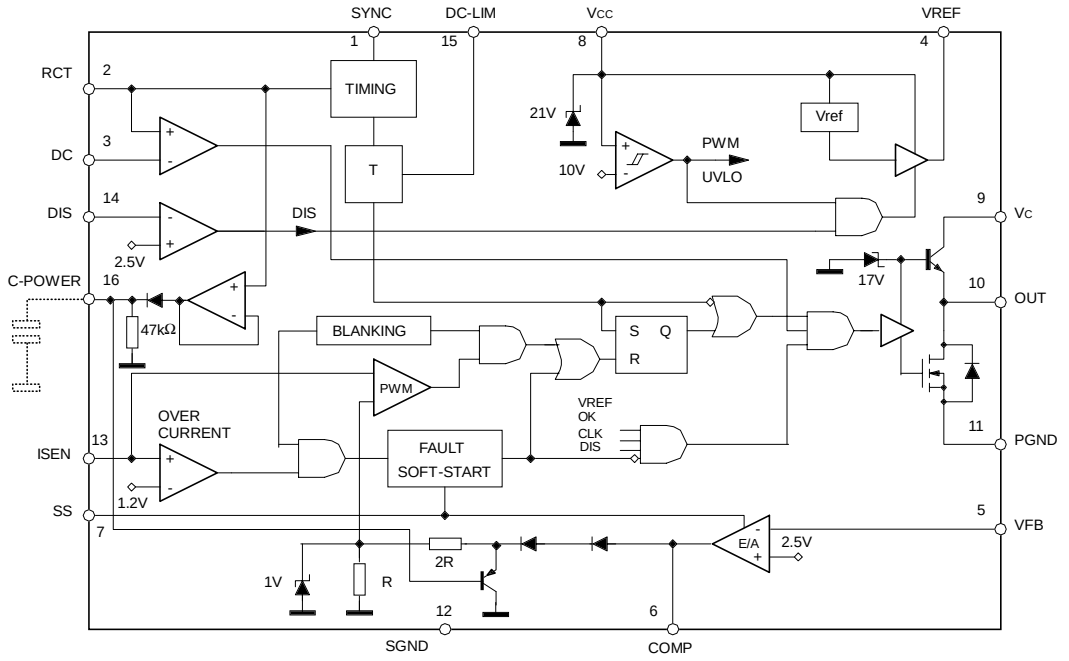

Fig. 12 - SGS-THOMSON's L5993 internal block diagram

Fig. 13 shows the detailed schematic of the current loop of the L5993 and the circuit relevant to the Constant Power function, where the frequency-to-voltage converter and the clamp can be easily picked out.

The real structure of the current loop is quite different from the equivalent one illustrated in fig. 1, and the Constant Power clamp has to act directly on the E/A output. The NPN-PNP pair on the (+) input of the PWM comparator corresponds to the two zero duty cycle diodes of the equivalent circuit and matches both the pair below the 15kΩ resistor and the one that represents the 1V clamp.

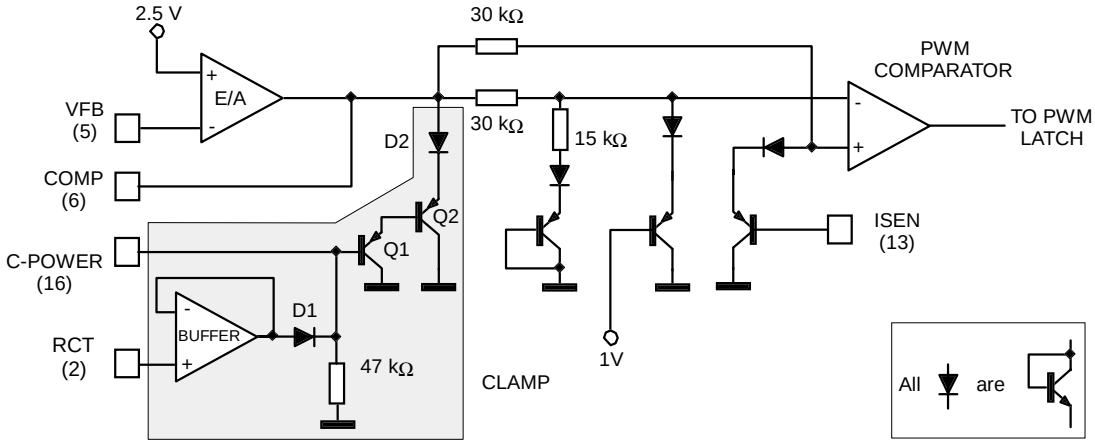

Fig. 13 - Constant Power Circuit detailed schematic

In order to guarantee a good precision of the Constant Power clamp circuit it is important to match the V_f of D1 and the V_{be} of Q1 so that the voltage on the base of Q2 is right the peak of the oscillator. It is obvious that also the pair D2-Q2 has to match the two “zero duty cycle” diodes.

Finally, what remains to verify is whether the circuit implements the ACL thoretically determined by equation (13). The results of the test, along with the theoretical values are shown in Tab. 4.

f_{sync}/f_{osc}	Theoretical ACL	Real ACL	% Difference
1	3.000	2.879	-4.2
1.5	2.480	2.445	-1.4
2	2.172	2.179	+0.4
2.5	1.969	2.000	+1.6
3	1.825	1.871	+2.4
3.5	1.719	1.773	+3.1
4	1.636	1.697	+3.6
4.5	1.571	1.636	+4.0
5	1.518	1.585	+4.3
5.5	1.474	1.544	+4.5
6	1.436	1.508	+4.7

Tab. 4 - Measured values of the ACL implemented by the L5993

The real ACL, analytically representable by the follwing best fit curve:

$$ACL \approx \frac{6 + 1.86 \bullet \frac{f_{sync}}{f_{osc}}}{1 + 1.73 \bullet \frac{f_{sync}}{f_{osc}}} \qquad (22),$$

differs from the theoretical expression (13) by less than ±5%.
The ratio between the actual maximum input power *Plim* and the desired limit $P_{in\max}$, resulting from the real ACL is shown in fig. 14, at minimum (solid line) and maximum (dashed line) V_E. The conditions are the same as the previous comparison ($n \bullet V_{out}$ = 100V, V_O = 0).

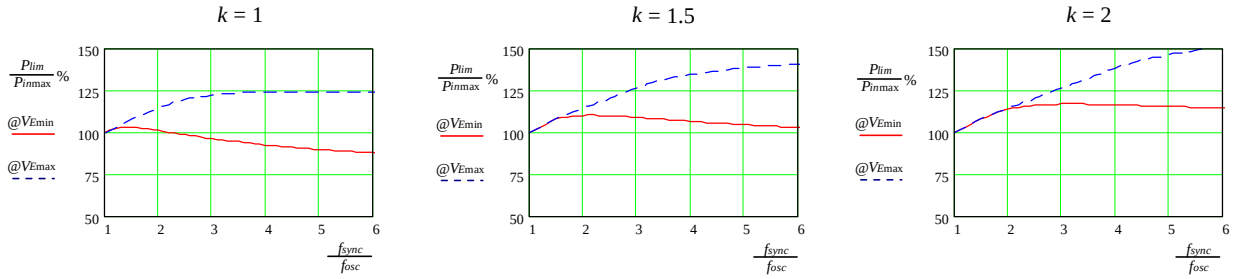

Fig. 14 - Comparison between ICL and the real ACL (Universal Mains)

It is worth noticing that the real ACL provides less than 3V @ f_{sync} / f_{osc} = 1. The value of R_S has been properly scaled so as to achieve 100% power capability in this condition.
As a result, it is obvious to suggest designing a flyback with *k* included between 1 and 2 in order to best fit ACL with ICL. Fortunately, this situation falls within those provided for by common design practice: the converter operates partly in CCM (at lower mains voltage and/or higher switching frequency) and partly in DCM (at higher mains voltage and/or lower switching frequency), what is sometimes called "Mixed Mode Operation".
The optimum value of *k*, however, depends on the specific application: input voltage range, reflected voltage, frequency range, oscillator free-running frequency are all parameters to be considered to this end. Also the margin of overload admitted (i.e. the ratio of the desired

capability limit $P_{in\max}$ and the input power at full load) should be taken into account: a reduction of this margin under certain conditions might be acceptable.
In addition, there is one more “tuning knob” that can be adjusted to better fit the real ACL with ICL: the offset voltage V_o. With a little overcompensation of the delay to output, that is by using an $R2/R1$ ratio (refer to fig. 5) slightly higher than what results from (12), combined with a fixed offset, it is possible to reduce the discrepancy at high V_E and high f_{sync} / f_{osc} and therefore to keep the $P_{lim} / P_{in\max}$ ratio closer to 1.

5 Conclusions

A method of controlling the throughput power of a current mode controlled flyback converter has been presented, called “Constant Power” function. It is based on a frequency-to-voltage conversion independent of amplitude and shape of the synchronization signal and on clamping the error amplifier output to this voltage.
It has been shown that the correction realized in this way is quite good and a PWM controller, SGS-THOMSON’s L5993, in which the Constant Power function is implemented has been introduced.

APPENDIX - Derivation of the Ideal Control Law and of Flyback's Power Capability

The Ideal Control Law (ICL) can be derived by the equation which describes the current loop:

$$V_C = 3 \bullet V_{csx} = 3 \bullet \left(R_s \bullet I_{px} + V_o \right) \quad \text{(A1)},$$

under the assumption that the delay to output of the PWM controller is compensated (so that V_O is an offset in addition to the one needed to do this). The expressions of the input peak current at the desired maximum input power $P_{in\max}$, considering DCM operation (that is, for $f_{sync} \le f_T$):

$$I_{px(DCM)} = \sqrt{\frac{2 \bullet P_{in\max}}{L_p \bullet f_{sync}}} \quad \text{(A2)}$$

and CCM operation (that is, for $f_{sync} \ge f_T$):

$$I_{px(CCM)} = \frac{P_{in\max}}{V_E} + \frac{V_E}{2 \bullet f_{sync} \bullet L_p} \quad \text{(A3)}$$

will be substituted in (A1) thus yielding:

$$V_{CLAMP} = \begin{cases} 3 \bullet \left(R_s \bullet \sqrt{\dfrac{2 \bullet P_{in\max}}{f_{sync} \bullet L_p}} + V_o \right) & , f_{sync} \le f_T \\ 3 \bullet \left[R_s \bullet \left(\dfrac{P_{in\max}}{V_E} + \dfrac{V_E}{2 \bullet f_{sync} \bullet L_p} \right) + V_o \right] & , f_{sync} \ge f_T \end{cases} \quad \text{(A4)},$$

being V_{CLAMP} the V_C voltage necessary to limit P_{in} to $P_{in\max}$ for any $f_{sync} > f_{osc}$. f_T is the transition frequency @$P_{in} = P_{in\max}$:

$$f_T = \frac{V_E^2}{2 \bullet L_p \bullet P_{in\max}} \quad \text{(A5)}$$

whose minimum value ($f_{T\min}$) occurs @$V_E = V_{E\min}$:

$$f_{T\min} = \frac{V_{E\min}^2}{2 \bullet L_p \bullet P_{in\max}} \quad \text{(A6)}.$$

This can be expressed in terms of the free-running frequency of the oscillator (f_{osc}):

$$f_{T\min} = k \bullet f_{osc} \quad \text{(A7)}.$$

The constant k will be assumed as a reference parameter, thus fixing k means fixing $f_{T\min}$ and, as a consequence the value of the primary inductance of the transformer (L_p). This can be found by combining (A6) and (A7) and solving for L_p:

$$L_p = \frac{V_{E\,\min}^2}{2 \bullet k \bullet f_{osc} \bullet P_{in\,\max}} \qquad \text{(A8)}$$

Equation (A8), which is a design equation, is substituted in (A4) thus yielding:

$$V_{CLAMP} = \begin{cases} 3 \bullet \left(R_s \bullet \dfrac{2 \bullet P_{in\,\max} \bullet \sqrt{k}}{V_{E\,\min}} \bullet \sqrt{\dfrac{f_{osc}}{f_{sync}}} + V_o \right) & , f_{sync} \le f_T \\ 3 \bullet \left[R_s \bullet \dfrac{P_{in\,\max}}{V_E} \bullet \left[1 + k \bullet \left(\dfrac{V_E}{E\,\min} \right)^2 \bullet \dfrac{f_{osc}}{f_{sync}} \right] + V_o \right] & , f_{sync} \ge f_T \end{cases} \qquad \text{(A9)}$$

The sense resistor Rs is selected so to ensure the desired capability $Pin_{\max}$ also when the input peak current is maximum, that is at minimum input voltage (i.e. @ $V_E = V_{E\min}$) and minimum operating frequency. Besides, it is desirable the variable clamp not to interfere with the 1V fixed clamp when the system is free-running, that is for $f_{osc} / f_{sync} = 1$.
Two cases are possible:

1) when the system, @ $f = f_{osc}$, operates in CCM ($\Rightarrow f_{osc} \ge f_{T\min} \Rightarrow k \le 1$);
2) when the system, @ $f = f_{osc}$, operates in DCM ($\Rightarrow f_{osc} \le f_{T\min} \Rightarrow k \ge 1$).

Therefore, by imposing $V_{CLAMP} = 3\text{V}$ in (A9), considering $f_{sync} = f_{osc}$ and $f_T = f_{T\min}$, and solving for Rs:

$$Rs = \begin{cases} \dfrac{(1 - V_o) \bullet V_{E\,\min}}{(1 + k) \bullet P_{in\,\max}} & , k \le 1 \\ \dfrac{(1 - V_o) \bullet V_{E\,\min}}{2 \bullet \sqrt{k} \bullet P_{in\,\max}} & , k \ge 1 \end{cases} \qquad \text{(A10)}\,.$$

Also (A10) is a design equation.
If the input power is fixed at $Pin_{\max}$, by dividing (A5) by (A6), it is possible to find that the transition frequency (f_T) at a certain equivalent voltage V_E and $f_{T\min}$ are related by:

$$f_T = f_{T\,\min} \bullet \left(\frac{V_E}{V_{E\,\min}} \right)^2 = k \bullet f_{osc} \bullet \left(\frac{V_E}{V_{E\,\min}} \right)^2 \qquad \text{(A11)}\,,$$

thus it is possible to write:

$$\begin{cases} f_{sync} \le f_T \Rightarrow \dfrac{f_{sync}}{f_{osc}} \le k \bullet \left(\dfrac{V_E}{V_{E\,\min}} \right)^2 \\ f_{sync} \ge f_T \Rightarrow \dfrac{f_{sync}}{f_{osc}} \ge k \bullet \left(\dfrac{V_E}{V_{E\,\min}} \right)^2 \end{cases} \qquad \text{(A12)}$$

Equations (A10) will be inserted into (A9) and the comparison between f_{sync} and f_T will be expressed as per (A12). Thus the final expression of ICL will be achieved:

$$V_{CLAMP} = \begin{cases} \begin{cases} 3 \bullet \left[\dfrac{2 \bullet (1 - V_o)}{1 + k} \bullet \sqrt{k \bullet \dfrac{f_{osc}}{f_{sync}}} + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \le k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \\ 3 \bullet \left[\dfrac{1 - V_o}{1 + k} \bullet \left(\dfrac{V_{E\min}}{V_E} + k \bullet \dfrac{V_E}{V_{E\min}} \bullet \dfrac{f_{osc}}{f_{sync}} \right) + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \ge k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \end{cases} & , \ k \le 1 \\ \begin{cases} 3 \bullet \left[(1 - V_o) \bullet \sqrt{\dfrac{f_{osc}}{f_{sync}}} + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \le k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \\ 3 \bullet \left[\dfrac{1 - V_o}{2 \bullet \sqrt{k}} \bullet \left(\dfrac{V_{E\min}}{V_E} + k \bullet \dfrac{V_E}{V_{E\min}} \bullet \dfrac{f_{osc}}{f_{sync}} \right) + V_o \right] & , \ \dfrac{f_{sync}}{f_{osc}} \ge k \bullet \left(\dfrac{V_E}{V_{E\min}} \right)^2 \end{cases} & , \ k \ge 1 \end{cases} \quad \text{(A13)}$$

The next step is to calculate the power capability of a flyback. More precisely, we will find the relationship between the desired maximum capability $P_{in\max}$ (@ $f = f_{osc}$ and $V_E = V_{E\min}$) and the actual power capability (P_{lim}) of a flyback in case the clamp voltage of the E/A is not the Ideal Correction Law (A13) but a generic value V_Z. V_Z can be either a constant (which is the case in the absence of any correction) or a function of frequency in case of ACL (theoretical or real).
The power capability is given by the following relationships:

$$P_{\lim} = \begin{cases} \dfrac{1}{2} \bullet L_p \bullet I_{px\max}^2 \bullet f_{sync} & , \ f_{sync} \le f_T \\ I_{px\max} \bullet V_E - \dfrac{V_E^2}{2 \bullet L_p \bullet f_{sync}} & , \ f_{sync} \ge f_T \end{cases} \quad \text{(A14)}$$

where $I_{px\max}$ is the maximum input peak current, which flows when the E/A output is saturated high and $V_C = V_Z$, and f_T is defined as:

$$f_T = \frac{V_E^2}{2 \bullet L_p \bullet P_{\lim}} \quad \text{(A15)}.$$

Solving equation (A1) for $I_{px\max}$:

$$I_{px\max} = \frac{V_Z - 3 \bullet V_o}{3 \bullet R_s} \quad \text{(A16)}$$

yields the expression of the peak input current. This, inserted into (A14) along with the expression of the primary inductance L_p given by (A8) in turn yields:

$$P_{\lim} = \begin{cases} \dfrac{1}{2} \bullet \left(\dfrac{V_Z - 3 \bullet V_o}{3 \bullet R_s} \right)^2 \bullet \dfrac{V_{E\min}^2}{2 \bullet k \bullet P_{in\max}} \bullet \dfrac{f_{sync}}{f_{osc}} & , \ f_{sync} \le f_T \\ V_E \bullet \dfrac{V_Z - 3 \bullet V_o}{3 \bullet R_s} - \left(\dfrac{V_E}{V_{E\min}} \right)^2 \bullet k \bullet P_{in\max} \bullet \dfrac{f_{osc}}{f_{sync}} & , \ f_{sync} \ge f_T \end{cases} \quad \text{(A17)}$$

Now the expressions (A10) of the sense resistor R_S will be inserted into (A16), thus furnishing the following expression for the ratio $P_{lim} / P_{in\max}$:

$$\frac{P_{\lim}}{P_{in\max}} = \begin{cases} \begin{cases} \left[\frac{V_Z - 3 \bullet V_o}{6 \bullet (1 - V_o)}\right]^2 \bullet \frac{(1+k)^2}{k} \bullet \frac{f_{sync}}{f_{osc}} & , f_{sync} \le f_T \\ \frac{V_E}{V_{E\min}} \bullet \left[\frac{V_Z - 3 \bullet V_o}{3 \bullet (1 - V_o)} \bullet (1+k) - k \bullet \frac{V_E}{V_{E\min}} \bullet \frac{f_{osc}}{f_{sync}}\right] & , f_{sync} \ge f_T \end{cases} & , \; k \le 1 \\ \begin{cases} \left[\frac{V_Z - 3 \bullet V_o}{3 \bullet (1 - V_o)}\right]^2 \bullet \frac{f_{sync}}{f_{osc}} & , f_{sync} \le f_T \\ \frac{V_E}{V_{E\min}} \bullet \left[\frac{2 \bullet (V_Z - 3 \bullet V_o)}{3 \bullet (1 - V_o)} \bullet \sqrt{k} - k \bullet \frac{V_E}{V_{E\min}} \bullet \frac{f_{osc}}{f_{sync}}\right], & f_{sync} \ge f_T \end{cases} & , \; k \ge 1 \end{cases} \qquad \text{(A18)}$$

Since P_{lim} is not constant (and therefore equation (A11) no longer applies) the relationship between the transition frequency (f_T) defined by (A15) and the minimum transition frequency $f_{T\min}$, defined as per (A6), becomes:

$$f_T = f_{T\min} \bullet \frac{P_{in\max}}{P_{\lim}} \bullet \left(\frac{V_E}{V_{E\min}}\right)^2 \qquad \text{(A19)}$$

In order to have an explicit expression of f_T, equations (A18) evaluated for $f_{sync} = f_T$, will be substituted in (A19), thus yielding:

$$f_T = \begin{cases} \frac{V_E}{V_{E\min}} \bullet \frac{6 \bullet (1 - V_o)}{V_Z - 3 \bullet V_o} \bullet \frac{k}{1+k} \bullet f_{osc} & , \quad k \le 1 \\ \frac{V_E}{V_{E\min}} \bullet \frac{3 \bullet (1 - V_o)}{V_Z - 3 \bullet V_o} \bullet \sqrt{k} \bullet f_{osc} & , \quad k \ge 1 \end{cases} \qquad \text{(A20)}.$$